	Type	L #	Hits	Search Text	DBs	Time Stamp
1	IS&R	L1	1	("6150184").PN.	USPAT	2002/04/01 12:56
2	IS&R	L2	1	("6090443").PN.	USPAT	2002/04/01 13:51
3	IS&R	L3	1	("6322849").PN.	USPAT	2002/04/01 13:56
4	IS&R	L4	1	("6316797").PN.	USPAT	2002/04/01 13:00
5	BRS	L5	419	(first adj2 anneal)	USPAT	2002/04/01 13:01
6	BRS	L6	32	5 and ((oxygen same (inert adj2 gas)))	USPAT	2002/04/01 13:05
7	BRS	L7	18	6 and (mixture)	USPAT	2002/04/01 13:29
8	BRS	L8	3	7 and (partial adj2 pressure)	USPAT	2002/04/01 13:29
9	IS&R	L9	0	("(second adj2 anneal)").PN.	USPAT	2002/04/01 13:57
10	BRS	L10	516	(second adj2 anneal)	USPAT	2002/04/01 13:58
11	BRS	L11	2	10 and (encapsulation adj2 layer)	USPAT	2002/04/01 14:01

DOCUMENT-IDENTIFIER: US 6316797 B1
TITLE: Scalable lead zirconium titanate(PZT) thin film material and deposition
method, and ferroelectric memory device structures comprising such thin film
material

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CLPR:
(32) The capacitor of claim 30, wherein the PZT material is between a bottom
electrode formed of a material comprising iridium and/or platinum, and a **top electrode formed of a material comprising iridium and/or iridium oxide**.

DOCUMENT-IDENTIFIER: US 6287637 B1
TITLE: Multi-layer approach for optimizing ferroelectric film performance

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DEPR:
In some cases, a lead-rich cap layer 18 is desirable to buffer film degradation
during subsequent CMOS processing. If used, the cap layer 18 is ideally sufficiently removed from the nucleation layer 14 to ensure that it does not influence crystal growth. The cap layer 18 is optimized for thickness and lead
content to ensure compatibility with top electrode 20. If desired, a multi-layer bottom electrode 12 consisting of platinum and iridium, and a multi-layer **top electrode 20 consisting of platinum and iridium oxide** can be
used. Other layers, such as titanium adhesion layers, can also be used. While
platinum is a preferred electrode material, other appropriate electrode materials known in the art can be used as described in the Background of the
Invention.

DOCUMENT-IDENTIFIER: US 6242299 B1
TITLE: Barrier layer to protect a ferroelectric capacitor after contact has been made to the capacitor electrode

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DEPR:
Finally in FIG. 1, a platinum top electrode layer 26 is sputter deposited to a thickness of about 1750 Angstroms. The bottom and **top electrode layers 22 and 26 can also be formed of other metals or conductive oxides such as iridium or iridium oxide,** if desired.

DOCUMENT-IDENTIFIER: US 6080499 A
TITLE: Multi-layer approach for optimizing ferroelectric film performance

---------- KWIC ---------

DEPR:
In some cases, a lead-rich cap layer 18 is desirable to buffer film degradation
during subsequent CMOS processing. If used, the cap layer 18 is ideally sufficiently removed from the nucleation layer 14 to ensure that it does not influence crystal growth. The cap layer 18 is optimized for thickness and lead
content to ensure compatibility with top electrode 20. If desired, a multi-layer bottom electrode 12 consisting of platinum and iridium, and a multi-layer **top electrode 20 consisting of platinum and iridium oxide** can be
used. Other layers, such as titanium adhesion layers, can also be used. While
platinum is a preferred electrode material, other appropriate electrode materials known in the art can be used as described in the Background of the
Invention.